WHAT IS CLAIMED IS:

1. A sense amplifier pulse shaper circuit, wherein the pulse shaper circuit generates a sense amplifier equalization control signal and a sense amplifier enable signal, the sense amplifier equalization control signal having a rising transition effectively earlier than the rising transition of the sense amplifier enable signal, the sense amplifier enable signal having a falling transition effectively earlier than the falling transition of the sense amplifier equalization control signal, and the sense amplifier equalization signal being discharged into the sense amplifier enable signal.

2. The sense amplifier pulse shaper circuit, as recited in claim 1, wherein the sense amplifier equalization control signal and the sense amplifier enable signal are substantially in-phase.

3. The sense amplifier pulse shaper circuit, as recited in claim 1, wherein the sense amplifier equalization control signal and the sense amplifier enable signal have a value opposing an input value.

4. The sense amplifier pulse shaper circuit, as recited in claim 1, wherein a slope of a transitioning edge of the sense amplifier enable signal varies from a slope of a transitioning edge of the sense amplifier equalization control signal.

5. An integrated circuit comprising:
an input node;
a first switch coupled to the input node;
a second switch coupled to the input node;
an impedance coupled to the first and the second switches; and
a sense amplifier equalization enable node for receiving a first signal and a sense amplifier evaluation enable node for receiving a second signal, the nodes coupled to the impedance and respective ones of the first and second switches, wherein a first transition of the first signal is effectively earlier than a first transition of the second signal and a

second transition of the second signal is effectively earlier than a second transition of the first signal.

6. The integrated circuit, as recited in claim 5, wherein a slope of a transitioning edge of the first signal varies from a slope of a transitioning edge of the second signal.

7. The integrated circuit, as recited in claim 5, wherein the first transition of the first signal is a rising transition, the first transition of the second signal is a rising transition, the second transition of the first signal is a falling transition, and the second transition of second signal is a falling transition.

8. The integrated circuit, as recited in claim 5, further comprising:
a sense amplifier coupled to the sense amplifier equalization enable node and the sense amplifier evaluation enable node.

9. The integrated circuit, as recited in claim 5, wherein the first transition of the first signal is based at least in part on the first switch.

10. The integrated circuit, as recited in claim 5, wherein the first transition of the second signal is based at least in part on the first switch and the impedance.

11. The integrated circuit, as recited in claim 5, wherein the second transition of the first signal is based at least in part on the second switch and the impedance.

12. The integrated circuit, as recited in claim 5, wherein the second transition of the second signal is based at least in part on the second switch.

13. The integrated circuit, as recited in claim 5, wherein the first switch is coupled to the power node.

14. The integrated circuit, as recited in claim 5, wherein the second switch is coupled to the ground node.

15. The integrated circuit, as recited in claim 5, wherein the first and second switches are complementary devices.

16. The integrated circuit, as recited in claim 15, wherein the first switch is a p-type transistor and the second switch is an n-channel transistor.

17. The integrated circuit, as recited in claim 5, wherein the impedance includes a first and a second device.

18. The integrated circuit, as recited in claim 17, wherein the first and the second devices are complementary devices.

19. The integrated circuit, as recited in claim 17, wherein the first device is a p-type transistor and the second device is an n-type transistor.

20. The integrated circuit, as recited in claim 5, wherein the first signal and the second signal are substantially in-phase.

21. The integrated circuit, as recited in claim 5, wherein the sense amplifier equalization control node and the sense amplifier evaluation enable node receive signals opposing an input signal.

22. The integrated circuit, as recited in claim 5, embodied in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit.

23. A method for operating a sense amplifier, comprising:

substantially matching delays of a first control signal, the first control signal for substantially turning on and substantially turning off an equalization of the sense amplifier and a second control signal, the second control signal for substantially turning on and substantially turning off the sense amplifier;

substantially turning off equalization of the sense amplifier before substantially turning on a sensing operation;

effectively turning off the sensing operation before effectively turning on the equalization of the sense amplifier; and

discharging the first control signal into the second control signal.

24. The method, as recited in claim 23, further comprising:

adjusting a slope of a transitioning edge of the control signal for turning on and turning off an equalization of the sense amplifier.

25. The method for operating a sense amplifier, as recited in claim 23, wherein the matching includes generating the control signals with a single driver.

26. The method for operating a sense amplifier, as recited in claim 25, wherein the single driver includes a first output node and a second output node.

27. The method for operating a sense amplifier, as recited in claim 23, further comprising:

matching a phase of control signals for turning on and turning off an equalization of the sense amplifier and substantially turning on and substantially turning off the sense amplifier.

28. The method for operating a sense amplifier, as recited in claim 27, wherein the equalization of the sense amplifier is active low.

29. The method for operating a sense amplifier, as recited in claim 27, wherein the sense amplifier turning on is active high.

30. The method for operating a sense amplifier, as recited in claim 26, wherein the first and second output nodes are coupled to an impedance.

31. The method for operating a sense amplifier, as recited in claim 26, wherein the first output node is coupled to a first switch.

32. The method for operating a sense amplifier, as recited in claim 26, wherein the second output node is coupled to a second switch.

33. The method for operating a sense amplifier, as recited in claim 27, wherein the equalization of the sense amplifier is a precharge.

34. An apparatus comprising:

means for substantially matching delays of a first control signal and a second control signal;

means for substantially turning off precharging of the sense amplifier before substantially turning on a sensing operation;

means for substantially turning off the sensing operation before substantially turning on the precharging of the sense amplifier; and

means for discharging the first control signal into the second control signal.

35. The apparatus of 34, further comprising:

means for adjusting a slope of a transitioning edge of the control signal for turning on and turning off an equalization of the sense amplifier.

36. The apparatus of 34, further comprising:

means for matching a phase of control signals for substantially turning on and substantially turning off a precharging of the sense amplifier and substantially turning on and substantially turning off the sense amplifier.

37. A method of manufacturing an integrated circuit comprising:

forming an input node;

forming a first switch coupled to the input node;

forming a second switch coupled to the input node;

forming an impedance coupled to the first and the second switches; and

forming a sense amplifier equalization enable node for receiving a first signal and a sense amplifier evaluation enable node for receiving a second signal, the nodes coupled to the impedance and respective ones of the first and second switches, wherein a first transition of the first signal is effectively earlier than a first transition of the second signal and a

second transition of the second signal is effectively earlier than a second transition of the first signal.

38. The method of manufacturing an integrated circuit, as recited in claim 37, further comprising:

forming a sense amplifier coupled to the sense amplifier equalization enable node and the sense amplifier evaluation enable node.